Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming FinFET devices, comprising:

forming a first fin structure, a source region, and a drain region in a first area of a wafer;

forming a second fin structure, a source region, and a drain region in a second area of the wafer;

forming a phosphosilicate glass layer on the first area and the second area, the phosphosilicate glass layer being formed adjacent to at least one of a top surface or a side surface of the first fin structure;

removing the phosphosilicate glass layer from the second area;

forming a boron silicate glass layer on the first area and the second area;

annealing the first area and the second area, the annealing causing the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causing the second fin structure, source region, and drain region of the second area to be doped with boron;

removing the boron silicate glass layer from the first area and the second area; and

removing the phosphosilicate glass layer from the first area.

2. (Original) The method of claim 1 wherein the forming a phosphosilicate glass layer on the first area and the second area includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

3. (Original) The method of claim 1 wherein the forming a boron silicate glass layer on the first area and the second area includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

4. (Original) The method of claim 1 wherein the first area is an N-channel area.

5. (Original) The method of claim 4 wherein the second area is a P-channel area.

6. (Original) The method of claim 1 wherein the removing a phosphosilicate glass layer from the second area includes:

masking the first area, and

etching the phosphosilicate glass from the second area.

7. (Currently Amended) A method for doping a fin structure and source and drain regions in FinFET devices, comprising:

forming a first glass layer on the fin structure and source and drain regions of an N-channel device and a P-channel device;

removing the first glass layer from the P-channel device;

forming a second glass layer on the fin structure and source and drain regions of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer; and

annealing the N-channel device and the P-channel device to uniformly dope the fin structure and to dope source and drain regions of the N-channel device and the P-channel device.

8. (Original) The method of claim 7 further comprising:

removing the second glass layer from the N-channel device and the P-channel device; and

removing the first glass layer from the N-channel device.

9. (Original) The method of claim 7 wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

10. (Original) The method of claim 9 wherein the forming a first glass layer on the N-channel device and the P-channel device includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

11. (Original) The method of claim 10 wherein the forming a second glass layer on the N-channel device and the P-channel device includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

12. (Original) The method of claim 7 wherein the removing the first glass layer from the P-channel device includes:

forming a mask on the N-channel device, and

etching the first glass layer from the P-channel device.

13. (Currently Amended) A method for doping fin structures in FinFET devices, comprising:

forming a first glass layer on the fin structures of a first area and a second area;

removing the first glass layer from the second area;

forming a second glass layer on the fin structures of the first area and the second area; and

annealing the first area and the second area to dope the fin structures of the first area and the second area, the annealing occurring prior to forming a gate electrode.

14. (Original) The method of claim 13 further comprising:

removing the second glass layer from the first area and the second area; and

removing the first glass layer from the first area.

15. (Original) The method of claim 13 wherein the first glass layer comprises phosphosilicate glass and the second glass layer comprises boron silicate glass.

16. (Original) The method of claim 15 wherein the first area is an N-channel area and the second area is a P-channel area.

17. (Original) The method of claim 13 wherein the forming a first glass layer includes:

depositing phosphosilicate glass to a thickness ranging from about 100 Å to about 500 Å.

18. (Original) The method of claim 17 wherein the forming a second glass layer includes:

depositing boron silicate glass to a thickness ranging from about 100 Å to about 500 Å.

19. (Original) The method of claim 13 wherein the annealing causes the fin structure in the first area to be doped with phosphorus and the fin structure in the second area to be doped with boron.

20. (Original) The method of claim 13 wherein the forming a first glass layer includes:

forming the first glass layer directly on the fin structures of the first area and the second area.